

<b>Notice of References Cited</b>	Application/Control No. 09/978,358		Applicant(s)/Patent Under Reexamination BROCK ET AL.	
	Examiner Mark Connolly		Art Unit 2115	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,515,530	02-2003	Boerstler et al.	327/291
*	B	US-6,566,918	05-2003	Nguyen, Andy T.	327/115
*	C	US-6,639,441	10-2003	Ono et al.	327/175
*	D	US-6,781,419	08-2004	Harrison, Ronnie M.	326/95
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Nelson Victor P. et al., Digital Logic Circuit Analysis and Design, 1995, Prentice-Hall Inc., pages 268-277
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.